REMARKS

In the Office Action, the Examiner rejected Claims 1-38 over the prior art, allowed Claims 39-41 and 43, and objected to Claim 42. More specifically, with respect to Claims 1-38, the Examiner rejected Claims 1, 2, 3, 6, 7, 14, 15, 28, 32 and 33 under 35 U.S.C. §102 as being fully anticipated by U.S. Patent 5,555,201 (Dangelo, et al.), rejected Claims 1, 8 and 9 under 35 U.S.C. §102 as being fully anticipated by U.S. Patent 5,251,159 (Rowson), and rejected all of Claims 1-38 under 35 U.S.C. §103 as being unpatentable over Dangelo, et al. in view of U.S. Patent 6,327,394 (Kash, et al.).

Applicants are herein amending Claim 1 to include the limitations of Claim 4, and are rewriting each of Claims 36 and 37 in independent form including the limitations of Claim 1. Claim 4 is being cancelled, and Claims 16, 17 and 20 are being amended to be dependent from Claim 1 instead of the now cancelled Claim 4. Also, editorial changes are being made to Claims 17, 19, 20, 21, 30 and 31, the dependency of Claim 22 is being corrected, and Claim 42 is being cancelled to reduce the number if issues in this case.

For the reasons discussed below, Claims 1-3 and 5-38 patentably distinguish over the prior art and are allowable. The Examiner is, thus, requested to reconsider and to withdraw the above-identified rejections of Claims 1-3 and 5-38, and to allow these claims.

The present invention, generally, relates to a method and system for visualizing internal operations of an integrated circuit. This visualization, in turn, may be used as an aid to the design, verification and test of integrated circuits. In this visualization, measured or simulated activity of the integrated circuit is obtained and visually expressed. In one embodiment, the

circuit activity representation is visualized as a simulation of optical emissions that are caused by the simulated activity.

The prior art does not disclose or suggest this type of circuit activity representation.

For example, Dangelo, et al. discloses visualizing the operation of a circuit by displaying simulation results, and, specifically, displaying results in a schematic diagram. This reference is primarily directed to logic simulation, and does not discuss, among other matters, visualization of measure data, animation of schematics, causal relationships, or photoluminescence modeling.

Rowson discloses a method and procedure for analyzing simulation results. Rowson does not address the issue of visualizing the causal relationship information about expressed device activity or the simulation of optical emissions.

Kash, et al. describes a procedure for processing time-resolved optical emission data. In this procedure, digitized waveforms are formed from optical emission data, and these waveforms are processed and the results of the processing are analyzed to determine a time delay between emissions from two locations in an integrated circuit. The procedure is very accurate, allows significant automation, and is useful in tests having high noise or low numbers of detected photons.

None of these references, however, discloses or suggests the feature, described in Claim 1, of visualizing the device activity representation as a simulation of optical emissions that occur as a result of the device activity.

As discussed in detail in the present application, this feature of the invention is of utility because it contributes to a design aid that is easy to visualize and interpret.

Because of the above-discussed difference between Claim 1 and the prior art, and because of the advantages associated with those differences, Claim 1 patentably distinguishes over the prior art and is allowable. Claims 2, 3, 5-35, and 38 are dependent from, and are allowable with, Claim 1.

Another important feature disclosed in the present application relates to the visualization of the causal relationship between specific types of inputs and the resulting device activity. For example, the present application teaches how to visualize the relationship between a test vector sequence applied to the device, and resulting device activity. In one embodiment of the invention, that visualization is used to determine effectiveness of the test vector.

Claims 36 and 37, which are now independent claims, describe this feature of the invention. In particular, Claim 36 describes the feature of comparing first and second representations to determine how well the test vector recreates the activity generated by an instruction trace. Claim 37 describes the feature of analyzing the device activity, caused by the test vector, to verify or debug that vector.

As it is believed the Examiner has recognized on page 8 of the Office Action, the above-discussed features are significant and not shown in the prior art.

In particular, as mentioned above, Dangelo, et al. discloses visualizing circuit operation. However, this reference does not teach visualization of, among other matters, causal relationships. Also, Kash, et al. discloses a procedure in which device activity is generated, but this reference does not disclose or suggest the procedures of Claims 36 or 37 for determining the effectiveness of the test vectors themselves.

In light of the above-discussed differences between Claims 36 and 37 and the prior art, and because of the advantages associated with those differences, Claims 36 and 37 patentably distinguish over the prior art and are allowable. The Examiner is, hence, respectfully asked to reconsider and to withdraw the rejection of Claims 36 and 37 under 35 U.S.C. §103, and to allow these claims.

For the reasons discussed above, the Examiner is respectfully requested to reconsider and to withdraw the rejections of Claims 1-3, 6-9, 14, 15, 28, 32 and 33 under 35 U.S.C. §102, and the rejection of Claims 1-3 and 5-38 under 35 U.S.C. §103, and to allow Claims 1-3 and 5-38. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully submitted,

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